Tutorial I: High-Speed Circuit Modeling and Design Using X Parameters*

Organizer and Speaker: Prof. Jose Schutt-Aine
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Abstract: The era of big data will lead to systems handling the transport of large amounts of information. Simulation techniques for the prediction of signal propagation in these environments have become a subject of increased interest over the past few years. Behavioral and macro-modeling techniques have been among the most popular methods used to predict the performance of these systems. Currently, IBIS model interpreters/generators are used to achieve a behavioral representation of nonlinear circuit blocks from their ports. However, when switching speeds increase, these models are no longer accurate.

The introduction of X parameters* has created new possibilities for the analysis of nonlinear behavior in high-speed circuits. The concurrent introduction of nonlinear vector network analyzers (NVNA) has reinforced the viability of the technique. X parameters represent a superset of the traditional scattering parameters and offer a mathematical foundation for the treatment on nonlinear network and components. This introduction presents a serious opportunity for the modeling and analysis of serial links.

In this tutorial, we review the fundamentals of X parameters as the nonlinear superset of S parameters and discuss techniques to generate the time-domain response of high-speed links. X parameters are first obtained in the frequency domain. We address the issues related to the steady-state simulation before looking into transient behavior. In particular, we explore the problem of Volterra series representation combined with machine learning techniques to construct powerful mathematical models for nonlinear circuits. A comparative study of different approaches and results is also given.

José E. Schutt-Ainé received the B.S. degree in electrical engineering from the Massachusetts Institute of Technology, Cambridge, in 1981, and the M.S. and Ph.D. degrees from the University of Illinois at Urbana-Champaign (UIUC), Urbana, in 1984 and 1988, respectively. From 1981 to 1983, he worked at the Hewlett-Packard Technology Center, Santa Rosa, CA, as an Application Engineer, where he was involved in research on microwave transistors and high-frequency circuits. In 1988, he joined the Electrical and Computer Engineering Department as a member of the Electromagnetics and Coordinated Science Laboratories, where he is currently involved in research on signal integrity for high-speed digital and high-frequency applications. He is a consultant for several corporations. His current research interests include the study of signal integrity and the generation of computer-aided design tools for high-speed digital systems. Dr. Schutt-Ainé was a recipient of several research awards, including the 1991 National Science Foundation (NSF) MRI Award, the NASA Faculty Award for Research in 1992, the NSF MCAA Award in 1996, and the UIUC-NCSA Faculty Fellow Award in 2000. He has received several publication awards including

the IEEE EDAPS- 2013 Best Paper and the IEEE-EPEPS-2014 Best Paper. He is an IEEE Fellow and is currently serving as Co-Editor-in-Chief of the IEEE Transactions on Components, Packaging and Manufacturing Technology (T-CPMT).

**X-Parameters is a Trademark of Keysight Technologies, Inc.*

Tutorial II. Achieving Power Integrity through a Systematic Physics-Based Design

Organizer: Prof. James L. Drewniak
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Abstract: Power integrity in high-speed digital designs is among the significant design challenges for high data rate and high speed systems. Best engineering practices for design of a power distribution network at the package and PCB level are well known. In practice this comes down to minimizing inductance over the current-draw path. However, there are many subtle design choices that can impact achieving a minimal power net voltage ripple or meeting a target impedance specification. In order to achieve a best design with or without constraints on some of these choices, a proven methodology for calculating the portions of inductance associated with particular geometry features is necessary, and a knowledge of inductance physics that can be exploited to achieve the design specification within a given stackup and a minimal number of decoupling capacitors.

A systematic methodology has been developed for PDN design and PI analysis that can readily identify a best design given typical design constraints. A method for PDN impedance calculation will be shown, and approach for achieving a target impedance will be given. If the target impedance specification is not met, the developed methodology can be used to immediately identify if specifications can be met with design modifications within the constraints, and provide directions in doing so in one or two iterations while avoiding trial-and-error simulations.

The three presentations in this half-day tutorial are:

1) **Power Integrity Concepts for Physics-based PDN Design**
   Prof. James L. Drewniak, Missouri S&T EMC Laboratory

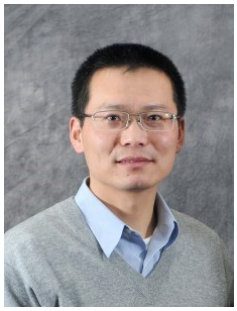
2) **A Pre-layout Design Approach for Achieving a Target Impedance**
   Prof. Jun Fan, Missouri S&T EMC Laboratory

3) **Low Inductance Decoupling Capacitor Interconnects and Library Models**
   Prof. Er-Ping Li, Zhejiang University

4) **Calculating Time-domain Noise Voltage for Power Integrity**

Prof. James L. Drewniak, Missouri S&T EMC Laboratory

James L. Drewniak is a Curator's Professor of Electrical and Computer Engineering at Missouri S&T. He received B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Illinois at Urbana-Champaign. His research is in electromagnetic compatibility, signal and power integrity, and electronic packaging. He is with the Electromagnetic Compatibility Laboratory, a university research laboratory of approximately 70 people that is internationally recognized for research in EMC and signal and power integrity. A key component of the research funding is the NSF Industry/University Cooperative Research Center (I/UCRC) for Electromagnetic Compatibility that is a consortium of approximately 20 companies. He is a Fellow of the IEEE, 2013 recipient of the IEEE EMC Society's Richard R. Stoddart Award, and a past Associate Editor of the IEEE Transactions on EMC.



Jun Fan (S'97-M'00-SM'06-F'16) received his B.S. and M.S. degrees in Electrical Engineering from Tsinghua University, Beijing, China, in 1994 and 1997, respectively. He received his Ph.D. degree in Electrical Engineering from the University of Missouri-Rolla in 2000. From 2000 to 2007, he worked for NCR Corporation, San Diego, CA, as a Consultant Engineer. In July 2007, he joined the Missouri University of Science and Technology (formerly University of Missouri-Rolla), and is currently a Professor and Director of the Missouri S&T EMC Laboratory. Dr. Fan also serves as the Director of the National Science Foundation (NSF) Industry/University Cooperative Research Center (I/UCRC) for Electromagnetic Compatibility and Senior Investigator of Missouri S&T Material Research Center. His research interests include signal integrity and EMI designs in high-speed digital systems, dc power-bus modeling, intra-system EMI and RF interference, PCB noise reduction, differential signaling, and cable/connector designs. In the IEEE EMC Society, Dr. Fan served as the Chair of the TC-9 Computational Electromagnetics Committee from 2006 to 2008, the Chair of the Technical Advisory Committee from 2014 to 2016, and a Distinguished Lecturer in 2007 and 2008. He currently is an associate editor for the IEEE Transactions on Electromagnetic Compatibility and IEEE EMC Magazine. Dr. Fan received an IEEE EMC Society Technical Achievement Award in August 2009.

Li Er-Ping is currently a Changjiang-Qianren Distinguished Professor, Dean of ZJU-UIUC Institute(Zhejiang University-University of Illinois at Urbana-Champaign), China. Prior that, he held various academic and managerial positions, he was the Department Director and Senior Director at A*STAR Institute of High Performance Computing, Deputy Dean to Faculty of Information Technology, Zhejiang University. He also served as Adjunct Associate Professor to ECE NUS from 2002-2008, Adjunct Professor to Peking University, Adjunct Professor at Applied Physics at NTU from 2012 to 2014 . Dr Li served the Global Advisory Panel to KAIST and External Academic Panel to City University of Hong Kong. Dr. Li is pioneering in applied electromagnetics and high speed electronics, he authored or co-authored over 400 papers published in the referred international journals and conferences, authored two books published by John-Wiley-IEEE Press and Cambridge University Press, holds and has filed a number of patents at the US patent office. He has been invited to give over 80 invited and keynote speeches at various international conferences and forums.

Tutorial III: Interconnect Characterization and IPC D24D Standard Development

Organizer: Prof. Jun Fan
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Abstract: High-speed interconnects are the enable technologies for emerging applications such as Internet of Things and cloud computing. With continuous increase of data rate, for example, an increase from 28 Gb/s to 56 Gb/s over a single lane for the next-generation 400 Gb/s Ethernet, power supply induced jitter (PSIJ) becomes an important player in determining the link quality, and thus needs to be addressed carefully. Noise and voltage fluctuations in the power distribution network due to device switching, if propagated to the I/O buffers, could result in jitter in the output waveforms. This power- and signal-net interaction is one of the aspects of Signal and Power Integrity co-design. In this workshop, analysis of PSIJ for I/O buffers are introduced from analytical formulations for simple single buffer structures, to extended approaches for buffer chains and complex I/O circuits.

Speaker: Dr. Xiaoning Ye
Affiliation: Intel Corporation, USA
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Xiaoning Ye received the Bachelor's and Master's degrees from Tsinghua University, Beijing, China, in 1995 and 1997, respectively, and the Ph.D. degree from the University of Missouri-Rolla (currently Missouri University of Science and Technology), Rolla, in 2000, all in electrical engineering. Dr. Ye joined Intel Corporation in 2001, and he is currently a Principal Engineer in Data Center Group, responsible for signal integrity of high speed interconnect. Dr. Ye holds eight patents and a few more patent applications in the areas of high-speed signaling. He is currently Vice Chair of the IEEE EMC Society Technical Advisory Committee, and Associate Editor of IEEE Transaction on EMC.

Speaker: Dr. Richard Zai
Affiliation: Packet Micro, USA
Contact information: rzai@packetmicro.com

Dr. Richard Zai is PacketMicro CTO and has more than 25 years of experience in architecting and delivering technology solutions in the areas of RF and signal integrity probing, wireless sensor networks, and radio frequency identification (RFID). In 1987, he joined IBM Watson Research Center as a research staff member and manager, where he pioneered in the development of RFID and high-speed robotic technologies. After leaving IBM in 1997, Richard co-founded start-up companies in Silicon Valley. Most recently, he has been leading the development of rugged 20-GHz test probes and patented probe stations that have been used by many Fortune 100 companies. Richard receives his Ph.D. degree from the University of Wisconsin-Madison and holds 15 US patents.

Speaker: Dr. Chunfei Ye
Affiliation: Intel Corporation, USA
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Dr. Chunfei Ye obtained B. Sci. in Mathematics from Hangzhou University in 1982, M. Eng from China Research Institute of Radiowave Propagation in 1985 and Doctoral Degree of Engineering in 1994 from Southeast University, both in EE. Before joining Intel China in 2002 as signal integrity (SI) and power integrity (PI) manager, Dr. Ye worked as a researcher with Shanghai Tiedao University, China, Institute of High Performance Computing, Singapore, and Massachusetts Institute of Technology, etc. He has been working with Intel Data Center Group since 2005 as SI tech lead, supporting all generations of Intel server PCH and SOC CPU package and platform signal integrity design. Dr. Ye serves as IEEE EMC-S TC 10 (SI and PI) Vice Chair

and IEEE EMC-S Distinguished Lecturer 2016-2017. He has published more than 50 papers on international conferences and journals and was granted 3 US patents.

Speaker: Mr. Jimmy Hsu
Affiliation: Intel Corporation
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Jimmy Hsu graduated from the electrical engineer department of national Chiao Tung University on 2000. He worked for Via technology from 2000 to 2008 and was in charge of SI/PI and EMI in Himax from 2008 to 2010. He joined intel as data center signal integrity to enable customer and innovation technology development.